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(71) Applicant *(for all designated States except US)*: **THE UNIVERSITY OF LIVERPOOL** [GB/GB]; Senate House, Abercromby Square, Liverpool L69 3BX (GB).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **ECCLESTON, William** [GB/GB]; 8 College Avenue, Formby, Merseyside L37 3JL (GB).

(74) Agent: **W.P. THOMPSON & CO.**; Coopers Building, Church Street, Liverpool L1 3AB (GB).

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(54) Title: A METHOD OF ELECTRONIC COMPONENT FABRICATION AND AN ELECTRONIC COMPONENT

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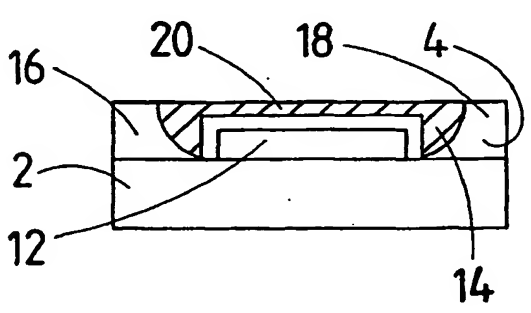

(57) Abstract: A method of fabricating an electronic component is disclosed in which an electrically conductive layer (4) is provided upon a substrate (2). A mask (6) having a window (8) is provided upon the conductive layer and by etching, preferably chemically, through the window an opening (10) is formed in the conductive layer. Conductive material is deposited, preferably by vapour deposition, through the window to form an island in the opening. The etching of the conductive layer is carried out such that the conductive layer is undercut at the periphery of the window with the result that the periphery of the island is spaced apart from the periphery of the opening. Also disclosed is a thin film transistor structure well suited to fabrication by the above described method.

DESCRIPTION

A METHOD OF ELECTRONIC COMPONENT FABRICATION AND AN ELECTRONIC COMPONENT

The present invention is concerned with a method of fabrication of an electronic component, and with an electronic component as such. The invention is in particular (although not exclusively) applicable to transistor fabrication, and still more particularly to fabrication of thin film transistors.

Considerable research effort has been devoted in recent years to thin film transistors (TFTs), and particularly to TFTs utilising bodies formed by thin films of semiconductor polymer. The TFTs so far proposed in the literature have been inverted horizontal structures. The gate is in most cases single crystal silicon which has been oxidised to produce a thin reliable oxide layer using a well defined technology, already available from work on silicon integrated circuits. An example of such a transistor is illustrated in schematic vertical section in Fig. 1, having a source 102 horizontally separated from a drain 104, both being formed above a gate 106 of silicon having an oxide layer 108 by which the gate is separated from the source and drain. The semiconductor body 110 is of polymer material.

A problem with the known horizontal TFT structures is that they have very large overlaps of the gate by the drain and source, as Fig. 1 clearly shows. In a typical inverter circuit, as used in digital applications, the drain voltage of the driver transistor is out of phase with that of the gate. This essentially doubles the magnitude of the voltage swing between these terminals. The same effect occurs with many

devices used in this configuration. It is called the Miller Effect and essentially doubles the effective overlap capacitance. The gate channel capacitance is one unit of capacitance, the source is a second and the drain is two units, making a total of four. Without the overlap capacitances there would be only one unit of capacitance, and a circuit utilising the transistor could go four times faster.

The silicon dioxide gate of the known TFT has a dielectric constant of 3.9. The amount of charge induced in the channel is proportional to this number. The gain obtained due to the gate's dielectric constant is countered by the Miller capacitance which makes the gate more difficult to drive. These effects exactly cancel.

There is, however, a benefit in use of a high dielectric constant material to isolate the gate, since it can allow a reduction in the threshold voltage of the transistor. The threshold voltage is the gate voltage required to turn on a channel. It is non-zero due to the undesirable effects of fixed charge in the oxide and any work function difference across the dielectric due to the materials used. These may serve to reduce threshold voltage for some kinds of devices.

There is a third effect, due to interface trapping levels, which always increases threshold voltage. This effect is very important in polymers so that there is great benefit in having a high gate dielectric constant.

Dielectric constant can vary from 1 to several hundred, but for most materials suitable for use in TFTs it is typically in the range 3 to 25. These are most likely to be the oxides of metals.

A major application of thin film polymer transistors is in flat panel displays. They are required to be very large in area so that the use of silicon is usually not feasible, and even if large area silicon were available the cost would be prohibitive. For most display applications the substrate material has to be transparent, making glass or plastic the favoured choice. There is therefore a need to limit the temperatures involved in manufacture to be compatible with such substrates. It is desirable that these temperatures should not be substantially greater than 200°C.

Efforts to reduce Miller capacitance have been limited by the dimensional tolerances in the processes used to fabricate horizontal component structures. In the known TFT, the gate and the source/drain are formed as successive layers using photolithographic techniques involving correspondingly formed resist layers, a first layer being used to form the gate and a further layer to form the source/drain. The accuracy of the relative lateral positioning of the gate and the source/drain is thus limited by tolerances in the formation of the resist layers themselves.

Hence a first object of the present invention is to make possible a method of electronic component fabrication having improved relative lateral positioning of two or more parts of the component.

The improvement is not only desirable in transistor manufacture but offers particular benefits in this area.

An additional or alternative object of the present invention is to make possible a transistor having reduced overlap capacitance.

An additional or alternative object of the present invention is to make possible

a transistor having a high gate dielectric content and particularly a gate dielectric constant higher than that of silicon dioxide. It is particularly desired to enable such a transistor to be fabricated without use of excessive temperatures.

It is further desired to achieve one or more of the above objects using a polymer based transistor, most preferably a thin film transistor.

In accordance with a first aspect of the present invention there is a method of electronic component fabrication comprising providing an electrically conductive layer upon a substrate; providing a mask over the conductive layer, the mask having at least one window; etching the conductive layer through the window to form an opening in the conductive layer; and depositing conductive material through the window to form an island in the opening, the etching being carried out such that the conductive layer is undercut at the periphery of the window so that the periphery of the island is spaced apart from the periphery of the opening.

By using the same mask window in forming the opening in the conductive layer and the island it becomes possible to determine the relative positioning of these two items with greatly improved accuracy not limited by the tolerance involved in manufacture of the mask itself. The undercutting of the conductive layer, which may for example result from use of a chemical etching process, is typically regarded as a problematic phenomenon, but is used to advantage in the method according to the present invention and makes it possible to ensure that despite being formed using a common mask the items are separated spatially - and if necessary also isolated electrically. Requiring only a single mask for fabrication of two or more parts, the

fabrication process according to the present invention is straightforward. Where the process is applied to transistor manufacture the island may form a transistor gate while separate portions of the conductive layer form the transistor source and drain. Gate isolation is, in a particularly preferred method according to the present invention, provided for by anodising the gate.

A metal gate is particularly preferred. Aluminium is a suitable material. The fabrication process can be carried out without excessively high temperatures and the resulting dielectric (metal oxide) layer can have the desired high dielectric constant.

Formation of the island is, in an especially preferred method according to the present invention, carried out by metal evaporation. The process can form an island whose periphery closely matches the periphery of the window.

In a particularly preferred method according to the present invention the transistor body is formed by introducing semiconductor material into the space between the island and the conductive layer. It is particularly preferred that the semiconductor materials comprises a polymer material. A suitable material is regio-regular polyalkylthiophene, although other polythiophenes are also suitable.

It is to be understood that the term "polymer" as used herein includes, as well as longer chain polymers, the relatively short chain oligomers.

In accordance with a second aspect of the present invention there is a thin film transistor comprising a source and a drain both substantially co-planar with and laterally separated from a gate, and a body comprising semiconductor material disposed between the source/drain and the gate.

This structure is well adapted to be fabricated by the method according to the first aspect of the present invention.

The source/drain and the gate may be co-planar in the sense that they are formed upon a common substrate.

It is especially preferred that the source/drain and the gate are formed using a common mask having a window, one being formed by etching through the window such as to undercut at the window periphery and the other being formed by deposition of material through the window.

The gate may be insulated from the body by a dielectric layer formed thereupon by selective anodisation.

Specific embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:-

Fig. 1 is a schematic vertical section through a conventional horizontal thin film transistor;

Figs. 2, 3, 4, 5, 6 and 7 are schematic vertical sections through successive stages in the production of a thin film transistor structure embodying the present invention, Fig. 6 illustrating the completed transistor.

The illustrated exemplary transistor embodying the present invention is formed on a substrate 2 of glass, although a plastics substrate - or indeed a substrate of some other material - may be used in other embodiments. At an early stage in the fabrication process (Fig. 2) a metal layer 4 is vacuum deposited upon the substrate and a photoresist layer 6 is spun upon the surface of the metal layer 4.

Subsequently a window is formed in the photoresist layer 6. In Fig. 3 this window is seen to take the form of an aperture 8 through the photoresist layer 6. The photoresist layer is thus adapted to serve as a mask for subsequent operations. The aperture 8 may be formed by conventional photolithography.

The metal layer 4 is then etched away chemically in the region determined by the aperture 8. It is important to note that the metal layer 4 is undercut around the periphery of the aperture 8 since the etch moves along the interface as well as downward through the metal. This type of undercutting is in itself known and understood. Those skilled in the art refer to the "etch factor" which is the allowance to be made in mask design for undercutting of the etched material. The result of the undercutting is that an opening 10 formed through the metal has somewhat larger horizontal extent than the mask aperture 8 used in its formation and that the etched metal edges have a concave curvature as Fig. 4 illustrates.

Metal is subsequently vacuum evaporated over the whole plate, reaching the glass substrate 2 only in the region of the aperture 8. In this way a metal island 12 is formed upon the substrate 2, within the opening 10, the island's horizontal extent more accurately matching that of the aperture 8 (see Fig. 5).

Due to the undercutting of the metal layer 4, there is a horizontal space 11 between this and the metal island 12. Because these parts are formed using the same mask aperture their relative positions are very accurately determined and the spacing can be kept to a minimum. Nonetheless, this spacing ensures that the metal layer 4 and island 12 are electrically isolated, making it possible to anodise the metal body

12 preferentially, eg. by plasma or aqueous anodisation. This requires an electrical connection to the metal island 12 which may be formed using elongate metal stripes leading to the edge of the substrate 2. The result of the anodising process is seen in Fig.6, the metal island 12 bearing on its exposed faces a dielectric layer 13 of anodised metal. Aluminium is a suitable metal for the island 12.

In Fig. 7. the resist layer 6 has been removed and conjugated semiconductor polymer material 14 has been cast across the surface, filling the void in the metal layer 4. Suitable semiconductor polymers are known to those skilled in the art. Regioregular polyalkylthiophene is used in the present embodiment.

The components of the transistor have now been formed. Source 16 and drain 18 are formed by portions of the metal layer 4; the gate is formed by the metal island 12 and is isolated from the semiconductor body, formed by the polymer material 14, by its anodised layer 13. This layer has, due to its material, the required high dielectric constant. The length of the transistor channel 18 is almost exactly equal to the dimension of the aperture 8 which was formed in the resist and can be made equal to the minimum feature size. Overlap of the source/drain with the gate is minimal.

CLAIMS

1. A method of electronic component fabrication comprising providing an electrically conductive layer upon a substrate; providing a mask over the conductive layer, the mask having at least one window; etching the conductive layer through the window to form an opening in the conductive layer; and depositing conductive material through the window to form an island in the opening, the etching being carried out such that the conductive layer is undercut at the periphery of the window so that the periphery of the island is spaced apart from the periphery of the opening.

2. A method of electronic component fabrication as claimed in claim 1, wherein chemical etching is used in forming the opening in the conductive layer.

3. A method of electronic component fabrication as claimed in claim 1 or claim 2 wherein formation of the island is by metal evaporation.

4. A method of electronic component fabrication as claimed in any preceding claim involving a further step of introducing semiconductor material into the space between the island and the conductive layer.

5. A method of electronic component fabrication as claimed in claim 4 wherein the semiconductor material is a polymer material.

6. A method of electronic component fabrication as claimed in claim 4 or claim 5 wherein the semiconductor material is a polythiophene.

7. A method of electronic component fabrication as claimed in claim 4, 5 or 6 wherein the semiconductor material is regioregular polyalkylthiophene.

8. A method of electronic component fabrication as claimed in any preceding

claim wherein the electronic component is a transistor.

9. A method of electronic component fabrication as claimed in claim 8 wherein the island forms a transistor gate and separate portions of the conductive layer form the source and drain.

10. A method of electronic component fabrication as claimed in claim 4 or claim 5 wherein gate isolation is provided by anodising the gate.

11. A method of electronic component fabrication as claimed in any preceding claim wherein the gate comprises aluminum.

12. A method of electronic component fabrication as claimed in any preceding claim wherein the substrate is transparent.

13. A method of electronic component fabrication as claimed in any preceding claim wherein the component is incorporated in a visual display.

14. A thin film transistor comprising a source and a drain both substantially co-planar with and laterally separated from a gate, and a body comprising semiconductor material disposed between the source/drain and the gate.

15. A thin film transistor as claimed in claim 14 wherein the source, drain and gate are formed upon a common substrate.

16. A thin film transistor as claimed in claim 14 or claim 15 wherein the gate is insulated from the body by a dielectric layer formed by anodisation of the gate.

17. A thin film transistor as claimed in claim 14, 15 or 16 wherein the semiconductor material comprises polymer material.

18. A thin film transistor as claimed in any of claims 14 to 17 wherein the

semiconductor material comprises a polythiophene.

19. A thin film transistor as claimed in any of claims 14 to 18 wherein the source/drain and the gate are formed using a common mask having a window, one being formed by etching through the window such as to undercut at the window periphery and the other being formed by deposition of material through the window.

20. A thin film transistor as claimed in claim 19 wherein the opening in the conductive layer is chemically etched.

21. A method of electronic component fabrication substantially as herein described with reference to and as illustrated in accompanying Figs. 2 to 7.

22. A thin film transistor substantially as herein described with reference to and as schematically illustrated in Fig. 7.

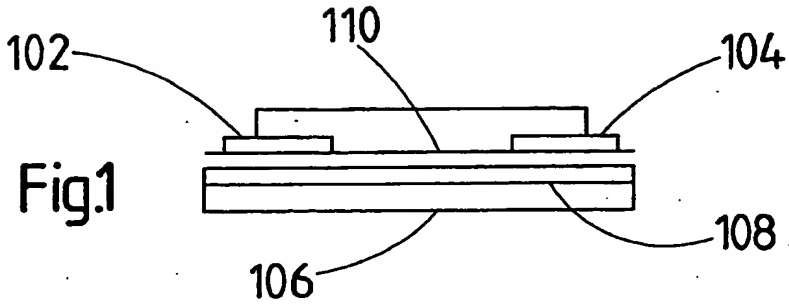

Fig.1

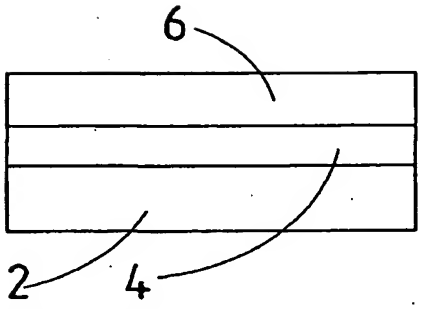

Fig.2

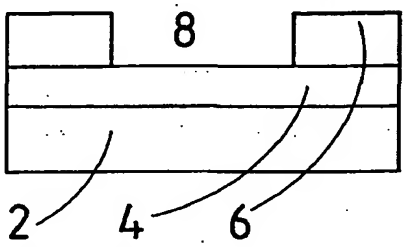

Fig.3

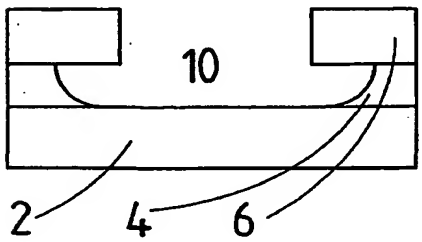

Fig.4

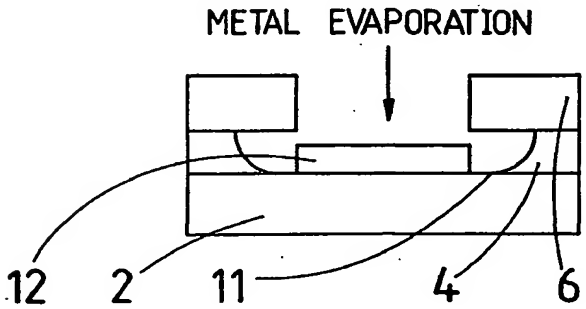

Fig.5

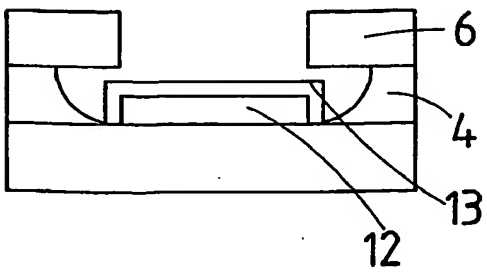

Fig.6

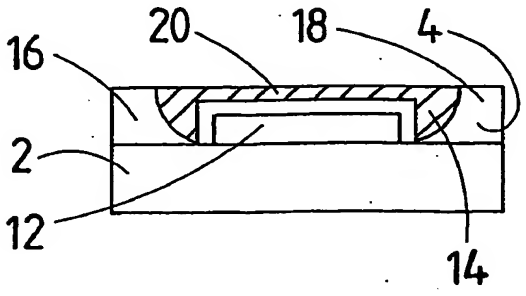

Fig.7

INTERNATIONAL SEARCH REPORT

Inte al Application No
PC /US 01/02456

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 585 655 A (OTA YORITO ET AL) 17 December 1996 (1996-12-17) column 6, line 22 - line 67 column 7, line 46 -column 9, line 9; figures 1A,3A,5A,6A,7AB,8	1-3,8,9, 11 14,15, 19,20
X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 613 (E-1458), 11 November 1993 (1993-11-11) -& JP 05 190856 A (SEIKO EPSON CORP), 30 July 1993 (1993-07-30) paragraph '0016! - paragraph '0033!; figure 1	14-16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 August 2001	23/10/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Micke, K

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Form PCT/ISA/210 (second sheet) (July 1992)

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 19-22

Claims 19,20:
The claims lack clarity since they constitute device claims, but the features claimed refer to a process.

Claims 21,22:
Claims relying on drawings (see PCT Rule 6.2(a)).

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

ormation on patent family members

Inte ial Application No
PC1/GB 01/02456

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5585655 A	17-12-1996	JP 8115924 A	07-05-1996
JP 05190856 A	30-07-1993	NONE	